

**REPORT OF
DEPARTMENT OF DEFENSE
ADVISORY GROUP ON ELECTRON DEVICES**

**EXTENDED
SPECIAL TECHNOLOGY AREA REVIEW
ON
HIGH-SPEED OPTICAL PROCESSING**



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PREFACE

DoD and NASA have underscored the need, in the next five to ten years, for military and space hardware that will perform at 10^{12} (tera) or greater operations per second (ops/s). Even though silicon technology has a strong commercial base, is technically very mature, and is progressing rapidly, performance of this scale, in the projected time frame, is considered a stretch for an all-electronic processor technology. As a consequence the Advisory Group on Electron Devices (AGED), Working Group C (Electro-Optics), held a review on high-speed optical processing (HSOP) to determine if optics might significantly extend the performance of electronic processors to tera ops/s. AGED and its Working Groups periodically undertake special technical areas reviews (STARs) that bring together industrial consultants and key military program managers to assess emerging device technology for possible exploitation in future military systems. The STARs play a significant role in the coordination of the military Service's present and future technical plans.

The STAR on HSOP was extended (XSTAR) both in depth and scope to allow government planning and funding officials to determine the potential benefits of this emerging technology, and to provide the details needed to assess the development of new technical opportunities for insertion in military systems.

The underlying questions posed by the HSOP XSTAR are:

- What is the rate of maturity of the emerging HSOP technology?
- How do performance projections match user requirements?
- How should future plans be formulated for HSOP?

At the outset, there was no clear approach to carrying out the XSTAR because addressing these questions in the broad context of "photonic" devices often obscured the dominant issues. By restricting the XSTAR to a few representative military systems, a proper focus was established to concentrate on the above basic questions.

The HSOP XSTAR involved continuous review, discussions, and interim summaries at six AGED Working Group C meetings. The editor wishes to thank all those who contributed to these meetings and particularly to Mr. William Miceli, ONR, who organized the speaker agenda to provide continuity and expert technical assistance. Special appreciation is expressed to Dr. Kermit Cuff who reviewed the final document. In addition, both the support and encouragement of Dr. John MacCallum, ODDDRE/R&AT/ET (Electronic Sensors and Devices), have been essential to this effort. There were 29 technical presentations, and more than 60 non-AGED attendees from 32 different organizations. This level of coordination and the resulting technical cross-fertilization was a major dividend of the XSTAR.

*Gerald Weiss
Palisades Institute
for Research Services, Inc.
(AGED Secretariat)
Arlington, VA*

CONTRIBUTORS

Dr. John M. MacCallum, Jr.
Executive Director, Advisory Group on Electron Devices
ODDDRE/R&AT/ET, The Pentagon
Washington, DC

Dr. Thomas Hartwick
Chairman, Working Group C (Electro-Optics)
TRW
Redondo Beach, CA

Dr. Ravindra Athale
BDM
McLean, VA

Dr. Paul Fletcher *
NOSC
San Diego, CA

Dr. Douglas Brown
NSA
Greenbelt, MD

Dr. Lynn E. Garn
C2NVEO
Ft. Belvoir, VA

Prof. John H. Caulfield
Center for Applied Optics
University of Alabama,
Huntsville, AL

Ms. Linda L Graceffo
C2NVEO
Ft. Belvoir, VA

Dr. Sen-Ti Chow
C2NVEO
Ft. Belvoir, VA

Dr. Peter Guilfoyle
OptoComp Corp.
Zephyr Cove, NV

Dr. Kermit F. Cuff *
Lockheed Missile and Space Co., Inc
Redondo Beach, CA

Mr. Brian Hendrickson
Rome Laboratory
Griffiss AFB, NY

Dr. Matthew Derstine
Boeing High Technology Center
Seattle, WA

Dr. Allen Huang
AT&T Bell Labs
Holmdel, NJ

Prof. Nabil Farhat
University of Pennsylvania
Philadelphia, PA

Dr. Albert Jamberdino
Rome Laboratory
Griffiss AFB, NY

* *AGED Working Group C (Electro-Optics)*

CONTRIBUTORS (CON'D)

Prof. Harry Jordan

*Center for Optoelectronic Computing
Boulder, CO*

Dr. Laveen Kanal

*LNK Corporation
Riverdale, MD*

Dr. Arthur Lockwood *

*Amber Engineering
Goleta, CA*

Dr. Fritz Kub

*NRL
Washington, DC*

Dr. Carl Magee *

*NASA
Hampton, VA*

Dr. John Malamas *

*C2NVEO
Fort Belvoir, VA*

Dr. Ellen Ochoa

*NASA Ames Research Center
Moffett Field, CA*

Mr. William Miceli *

*ONR
Boston, MA*

Dr. Ronald Paulson *

*EDO Corporation
Barnes Engineering Division
Shelton, CT*

Mr. Richard Payne *

*Rome Laboratory
Hanscom AFB, MA*

Dr. John Pellegrino

*HDL
Adelphi, MD*

Dr. Robert Rediker *

*Lincoln Laboratory, MIT
Lexington, MA*

Dr. Steven Sawtelle

Wright Patterson AFB, OH

Dr. Anthony Spezio

*NRL
Washington, DC*

Mr. Bernie Soffer

*Hughes Research Lab.
Malibu, CA*

Mr. Greg Swietek

*NASA HQ
Washington, DC*

Mr. Joseph Swistak

*C2NVEO
Ft. Belvoir, VA*

Prof. Anthony Vanderlught

*North Carolina State
Raleigh, NC*

Prof. Kelvin Wagner

*University of Colorado
Colorado Springs, CO*

Dr. Richard Williamson

*MIT/Lincoln Lab
Lexington, MA*

Mr. Fred Walters

*ONR
New York, NY*

Dr. Andrew C. Yang

*DARPA
Arlington, VA*

*AGED Working Group C (Electro-Optics)

CONTENTS

I. OVERVIEW OF REPRESENTATIVE SYSTEMS

| | | |
|-----|--|----|
| A. | Introduction | 1 |
| B. | Computational Requirements for Future Military Hardware | 1 |
| B.1 | Electronic Warfare and Electronic Intelligence | 2 |
| B.2 | Automatic Target Recognition | 4 |
| B.3 | Antisubmarine Warfare | 8 |
| B.4 | Multispectral Analysis | 11 |
| B.5 | Applications Requiring High-Speed Switching and Connectivity | 14 |
| C. | Optical Versus Electronic Interconnections | 16 |
| D. | Optical Versus Electronic Memory Capability | 19 |
| E. | Compact Spatial Light Modulator - A Critical Component | 22 |

II. WHAT MAKES OPTICAL PROCESSING DESIRABLE?

23

III. *TECHNOLOGY PUSH* AND *SYSTEMS PULL* OF HSOP

24

IV. GOVERNMENT-SUPPORTED PROGRAMS IN HSOP FOR FY 1990

25

V. U.S. VERSUS FOREIGN EFFORT IN HSOP

27

VI. TECHNICAL ASSESSMENT

28

CONTENTS (CON'D)

Tables

| | |
|--|----|
| I. Comparison Of The Performance Of BPOF Optical Correlator And Electronic Implementation | 7 |
| II. Vertical Cavity SEL Performance | 19 |

Figures

| | |
|--|----|
| 1. Acousto-Optic Heterodyne Spectrum Analyzer | 3 |
| 2. Signal Collection: Front-End Requirements Versus Device Capability | 4 |
| 3. Optical Image Correlation Architecture | 5 |
| 4. Effects Of Clutter On Correlator Performance | 7 |
| 5. Symmetric Self-Electro-Optic Effect Device (S-SEED) | 9 |
| 6. Projected Performance Of S-SEEDs | 10 |
| 7. Computational Requirements Of ASW | 11 |
| 8. Typical NASA Mission Requirements Versus Optical Capability | 12 |
| 9. Three-Layer Artificial Neural Network | 13 |
| 10. Optical Switch Device Capability | 15 |
| 11. Power Requirements For Digital Interconnections | 17 |
| 12. A SEL Array Optical Matrix Processor | 18 |
| 13. A Typical Vertical Cavity SEL Structure | 18 |
| 14. Memory Capacity Versus Access Time | 20 |
| 15. Compact SLM Projected Capability For Optical Correlators | 23 |
| 16. HSOP Application Perspective | 25 |
| 17. Government-Supported Programs In HSOP For FY 90 | 26 |
| 18. Qualitative Assessment Of The Relative Level Of Effort In HSOP: U.S. Versus Foreign | 27 |

I. OVERVIEW OF REPRESENTATIVE SYSTEMS

A. Introduction

Silicon electronic processors are at the heart of all modern DoD systems and each year great strides are made in improving performance. With the VHSIC II program completed, the last concerted effort to increase chip functionality is nearly ended and insertion of this technology into systems is proceeding. As part of this thrust, the development of the next generation high-speed processor was initiated by the DARPA Touchstone program. In this development, optics is seriously considered as the high-speed optical reconfigurable interconnect that will provide microelectronic system architectures with additional processing functionality. Other examples that have capitalized on optics in niche applications are one-dimensional (1D) channelizers, synthetic aperture radar (SAR) post-processors, and optical correlators.

To shed further light on the potential of HSOP as a complement to silicon technology, this report summarizes the requirements for five representative systems whose operation is projected to be computationally intensive. The prominent emerging optical devices that have the greatest potential to satisfy these requirements are also presented. The applications are divided into four DoD systems: electronic warfare (EW), electronic intelligence collection (ELINT), automatic target recognition (ATR), and antisubmarine warfare (ASW); and in addition NASA system requirements. These system requirements are important because they tax the limits of today's technology relative to incremental improvements projected into the future. The limitations take various forms; for example, the false-alarm rate for ATR is too high or the throughput rate for a vector processor begins to require parallel combinations of processors as opposed to an increase in the functionality of an existing processor subsystem, etc. Basically, the underlying issue is that military requirements will need a two-orders-of-magnitude increase in computing power from about 10^{10} ops/s to about 10^{12} ops/s in the next five years.

B. Computational Requirements For Future Military Hardware

It is projected that the military Services will require a substantial increase in computing power to satisfy advanced battlefield, avionic, and naval operations in EW, ELINT, ATR, and ASW. In addition, an enhanced computational capability will be vital to NASA in the development of hardware for automated object recognition in satellite docking, maintenance and repair, and multispectral analysis.

The emerging technology of HSOP has the potential to meet these future military and NASA needs because experimental and prototype hardware have already shown that optical subsystems significantly improve the operational capability of many military systems. In these new developments, EW and ELINT hybrid optical/electronic architectures have resulted in smaller and more efficient hardware with greater sensitivity to the enemy threats contained within the dense electromagnetic (EM) environment of exotic signals. Also, laboratory demonstrations of optical subsystems in ATR hardware show a better operational capability compared to an all-electronic approach. In addition to these potential applications, the success of these research programs indicate that a hybrid of optical/electronic hardware can satisfy a specific future computational ASW demand.

B.1 Electronic Warfare and Electronic Intelligence

EW and ELINT military systems must be able to quickly pick out enemy threats from the dense EM environment of combined enemy signals, EM interference, and friendly radiation sources, and must be able to react to these threats with a warning alarm, an EM countermeasure, or a "hand off" to a weapon system. The success of EW battle responses not only depends on reducing the reaction time to the threat, but also requires minimizing the number of false and undetected threats. To do this effectively, the hardware must have a computational capability to reliably sort out and analyze such diverse enemy signal parameters as the instantaneous frequency, phase, polarization, direction of arrival, time between pulses, scanning rate, etc. To meet future military needs, it is necessary that these signal parameters be determined in "realtime."

The intrinsic parallelism of optics will be able to satisfy the high computational rate needed for these future military systems. For signal collection applications, a hybrid optical/electronic architecture has evolved that consists of a receiver "front end" to detect the EM environment and produce an intermediate frequency (IF) output, an optical subsystem to channelize the IF signal spectrum to a number of photodetector outputs, and an electronic "back-end" processor to format the photodetector output into a threat analysis for display or an automatic action. The process of generating the spectral power density of the wideband input signal is performed by the optical subsystem which consists of a laser source to illuminate either a surface acoustic wave (SAW) or an acousto-optic (AO) cell, one-dimensional (1D), spatial light modulator (SLM), and a photodiode array that converts the resulting optical signals to an electronic signal for further post-processing.

The layout of an optical subsystem architecture is shown in Figure 1. As indicated in the figure, a piezoelectric transducer changes the time-varying IF signal to an acoustic strain wave that travels along a transparent AO cell which is generally fabricated from either lithium niobate, tellurium dioxide, or gallium phosphide material. The resulting strain wave spatially alters the index of refraction along the path of propagation to form a diffraction grating that modulates a laser beam passing through the material. The IF signal is therefore converted to a function of space and time and the resulting diffraction grating interacts with the incident laser beam to create the computational analog of taking the Fourier transform of the IF signal to produce its spectral power density. The most efficient interaction takes place when the angle between the incident laser wavefront and the acoustic wavefront is oriented at the Bragg angle.

In the conventional optical architecture, the transformed IF signal is directly detected by an array of photodiodes. The configuration of Figure 1 illustrates the use of a heterodyne-detection technique based on a newly developed optical architecture that greatly improves EW performance. In this approach, the signal-to-noise ratio is larger than that achieved by direct-detection because the signal from the Bragg cell is combined with a reference signal to form a beat signal that is much stronger than the photodetector noise. This architecture is now being used extensively in the class of hardware called AO spectrum analyzers and is implemented to perform EW or ELINT functions. As more of the EM spectrum is used for greater signal sophistication, it is projected that unless higher speed computational devices are developed, it will become more difficult to meet future EW and ELINT demands.

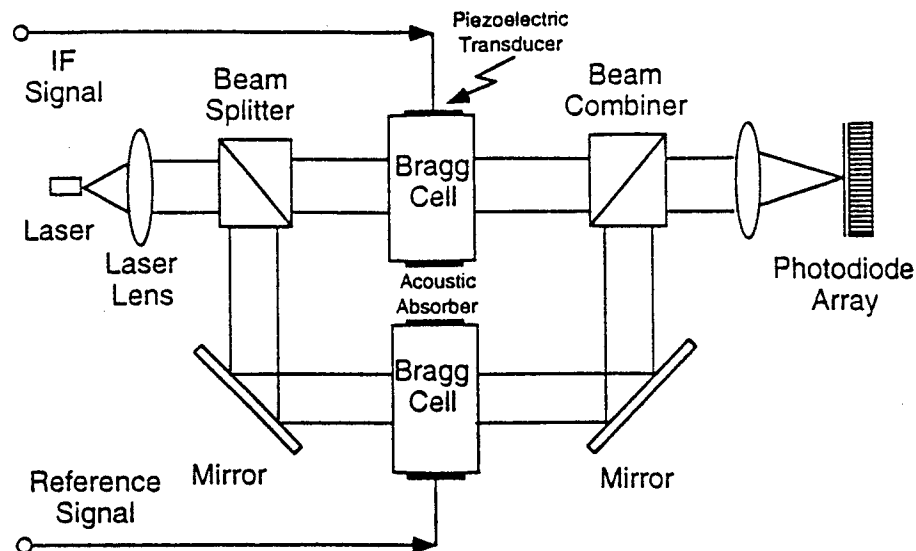


Figure 1 Acousto-Optic Heterodyne Spectrum Analyzer

EW electronic hardware now use 1D SLM optical subsystems to sort out the wideband instantaneous frequency of enemy signals into 20-MHz-wide channelized outputs. The front-end functions are performed by microwave and millimeterwave integrated circuit (MIMIC) technology, and the back-end digital processing is done by conventional very-large-scale-integration (VLSI) silicon chips that operate at one-giga operation per second (GOPS). Combining optics with electronics in a hybrid architecture promises to provide these military hardware with a large computational capacity in a small volume for less electrical input power compared to all-electronic hardware. The performance of these systems is generally expressed in terms of the instantaneous bandwidth of the EM environment and the dynamic range of the signal strengths that must be detected under battle conditions. Current EW applications typically processes a relatively large instantaneous bandwidth (about 1 GHz), at moderate dynamic range, to satisfy threat warning functions. ELINT, on the other hand, requires lower instantaneous bandwidth with large dynamic range (about 60 dB) to ensure that weak enemy signals are undistorted for precise analysis.

Figure 2 illustrates the computational requirements placed on military EW and ELINT systems to meet enemy threats in the period from 1990 to 1995. Superimposed on the graph are the performance curves of 1D SAW/AO SLMs identified to meet these system requirements. These projections are based on future needs of military EW systems to process the additional spatial and temporal enemy signal parameters with improved response time performance, false alarm rate, missed threats, and generic threat identification. It is apparent that an increased computational capability will be needed to satisfy an instantaneous bandwidth of up to 10 GHz and a dynamic range up to 65 dB. Similar computational demands will be made on ELINT systems in order to improve the dynamic range to 80 dB and an attending increase of instantaneous bandwidth to 1 GHz. The performance of SAW and AO devices are steadily improving and should meet these system requirements in the near term. Improved performance will be obtained in transitioning from conventional direct-detection

techniques, which limits dynamic range to about 40 dB, to the newer heterodyne-detection architectures.

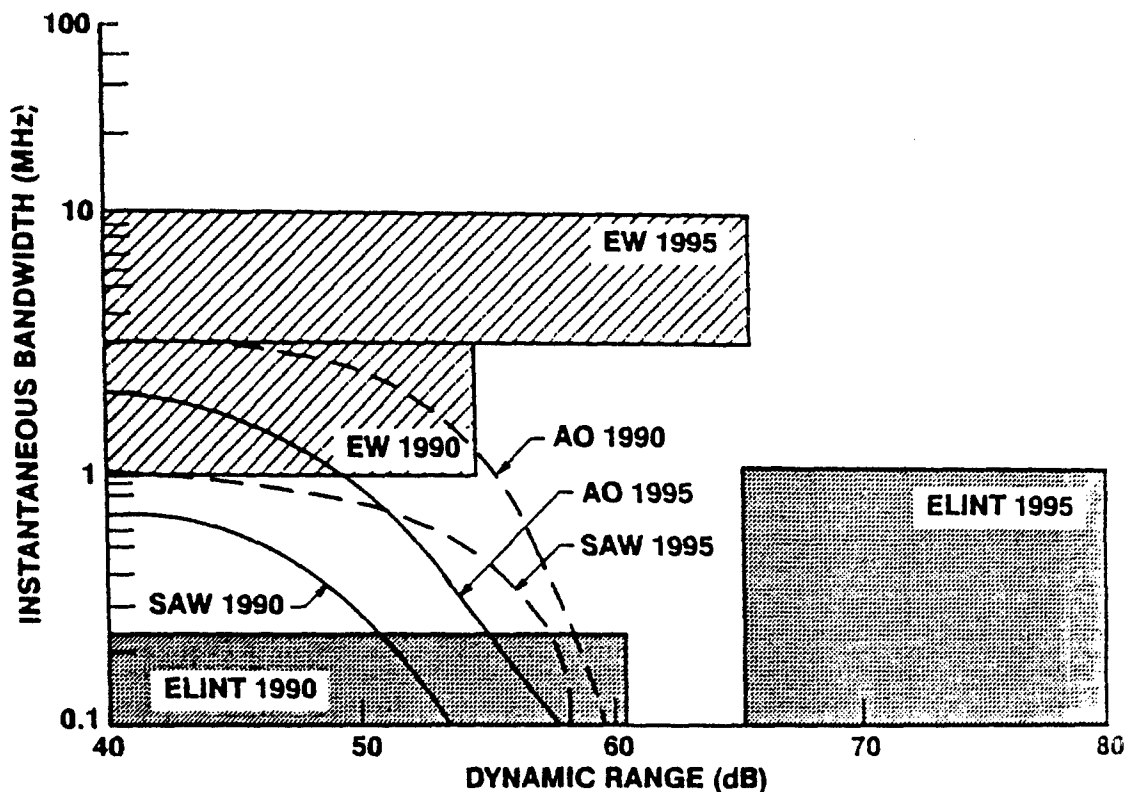


Figure 2 Signal Collection: Front-End Requirements Versus Device Capability

B.2 Military Hardware for Automatic Target Recognition

The military Services have been developing hardware to automatically recognize - under battle conditions - missiles, aeroplanes, tanks, jeeps, and soldiers in the field. This capability has a wide range of applications that include automated-second-pilot functions in aircraft, sensing aids in unmanned air vehicles, and tank target identification. NASA is also developing hardware for a variety of uses such as the automatic recognition of objects to assist in satellite docking.

Machines that recognize two-dimensional (2D) images of objects try to match an input image with a library of images stored in the machine. For military effectiveness, the machine must be able to rapidly compare specific types of objects in a composite scene that contains other background objects and natural non man-made clutter. In addition, successful comparison must not depend on the orientation of the object or the distance of the object to the recognition machine. It has become evident that a computational burden will be placed on the design of such systems that have to rapidly respond to enemy threats in a wide range of operational scenarios.

A standard approach to reduce the computational details of image matching is not to compare the actual input image with the library of stored images, but rather to compare the Fourier transform of the image with a stored reference. This technique is used because in the Fourier plane, the large spatial frequencies needed for image identification can be easily differentiated from the unwanted background clutter. Also, the Fourier transform of the image of an object is invariant to translation of the object in the scene and therefore the transform process reduces one of the variables of recognition.

New computational 2D architectures are being developed to capitalize on the parallelism of optics to more rapidly generate the analog of the Fourier and inverse Fourier transform used in the image correlation process. Optical subsystems using these techniques will be incorporated into military hardware and will significantly enhance future electronic ATR capabilities. This transition will occur because it has already been demonstrated that hybrid ATR systems composed of electronic and optical modules perform better than all-electronic systems.

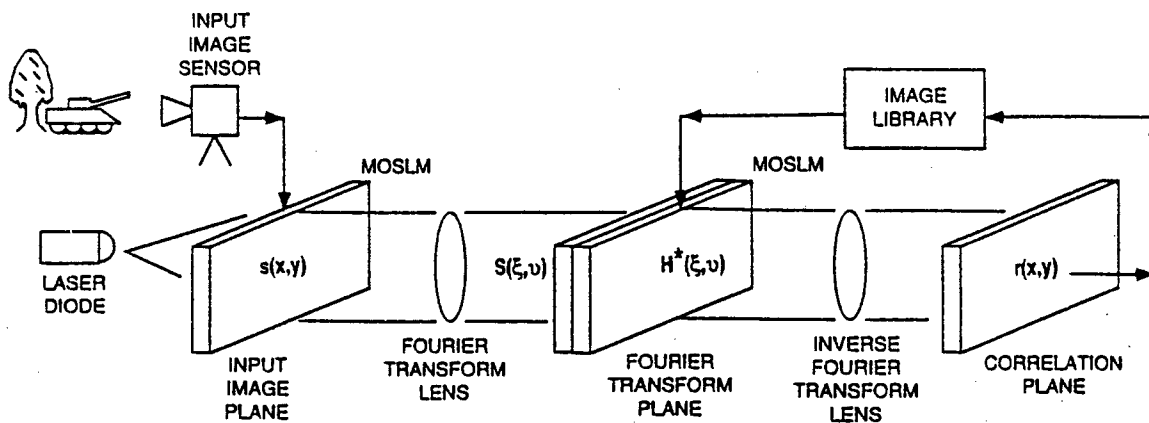


Figure 3 Optical Image Correlation Architecture

Figure 3 shows the use of an electronically addressed 2D magneto optic spatial light modulator (MOSLM) in an optical architecture that performs the optical correlation process. The MOSLM consists of a 2D thin film array of single crystal bismuth-substituted iron garnet addressable pixels. The polarization of a laser beam passing through each pixel is controlled by the Faraday rotation effect. As a result, the plane of polarization of the linearly polarized laser beam is rotated clockwise or counterclockwise, depending on the magnetization state of the pixels. This action turns the laser beam either "on" or "off." The control of the direction of magnetization of each pixel is done in three steps. First, a large external magnetic field is applied to the entire array to "erase" the magnetization state of all the pixels of the array. Next, the magnetization state of selected pixels is partially reversed by passing a current through the conductors that intersect the corners of the pixel.

Then, the selected pixels are driven to a saturation state by the application of the external field in a direction opposite to that used to erase the SLM.

In the application illustrated in the figure, the output of the image sensor produces a 2D spatial distribution $s(x,y)$ of the image of the object on the transparent MOSLM located at the input image plane. The parallel rays of coherent radiation from the laser diode source pass through the input image plane and the Fourier transform lens to generate at the second MOSLM the Fourier transform $S(\xi,v)$ of the input scene. The optical architecture is arranged so that one member of the library of the conjugate Fourier transform of stored images $H^*(\xi,v)$ is also formed at the second MOSLM. The analog of the product of $S(\xi,v)$ and $H^*(\xi,v)$ is produced at this plane and the spatial correlation function $r(x,y)$ is generated at the correlation plane by the inverse Fourier transform lens. The optical correlator process involves scanning the image library while looking for a peak response in the correlation plane. Successful correlation occurs when the largest peak in the correlation plane matches the Fourier transform of the correct image of the object stored in the library.

The library of the Fourier transform of stored images of objects $H^*(\xi,v)$ is composed of an amplitude and phase spectral function. Research workers in this field have recognized that the essential correlation information in a coherent optical image is contained in the phase function and hardly at all in the amplitude function. The potential for using optical correlation for pattern recognition was pioneered by Horner and Gianino in a 1984 paper on "Phase-Only Matched Filters," published in *Applied Optics* volume 23, page 812. In a computer simulation it was demonstrated that a phase-only matched filter, with the amplitude transmission set to unity, not only produces an acceptable correlation, but also results in better power throughput, a narrower and taller correlation response, and improved signal-to-noise ratio. The concept was subsequently extended to binarized phase with no degradation in performance, and was demonstrated experimentally using a binary-phase-only filter (BPOF).

Figure 4 illustrates the use of these techniques to increase the performance of recognizing an object in clutter. It can be seen that a pronounced peak in the correlation plane represents a considerable improvement compared to the response using a conventional matched filter.

MOSLM arrays are commercially available with 256×256 pixels and operate at a frame rate of 500 per second. Additional recent work has shown that a drastic reduction in data requirements results from optical correlation using the BPOF. In a laboratory test of an ATR system that used a Litton-Sematex MOSLM, the potential for realtime pattern (or target) recognition using a small digital computer was demonstrated -- something previously not possible. This improved ATR capability will shortly be exploited in a joint Air Force (RL) and Army (MICOM) effort funded by DARPA in which a brassboard device will be field tested. Further comparisons of the electronic state-of-the-art with a version of the BPOF correlator built by Litton was conducted by the Army Night Vision Laboratory and showed greatly superior performance of a hybrid approach. The results are summarized in Table I. The current and projected capability of the SLM for optical correlation is also shown. It is clear that ferroelectric liquid crystal and deformable micro mirror technology should have a distinct advantage over the MOSLM for this application.

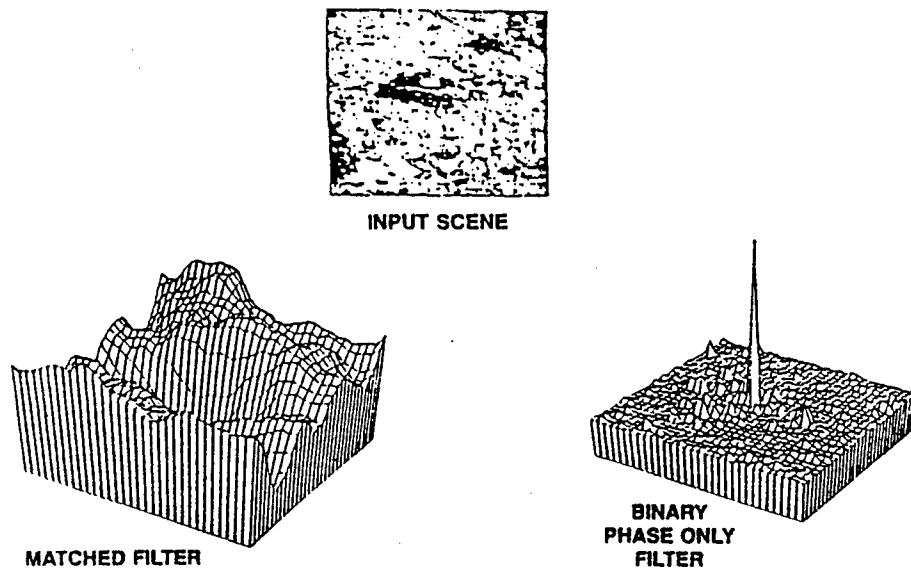


Figure 4 Effects Of Clutter On Correlator Performance

| | OPTICAL | DIGITAL |
|-------------------|------------------------------|-----------------------------|
| • SUCCESS RATE: | 90% | 33% |
| • DATA RATE: | 500 MOPS, PROJECTED 100 GOPS | 100 MOPS, PROJECTED 10 GOPS |
| • SOFTWARE NEEDS: | MINIMAL | CRITICAL |
| • SIZE: | ~0.01 m ³ | 2 m ³ |

| | PERFORMANCE | |
|-----------------------|---------------------|--------------------|
| | PRESENT | NEAR FUTURE |
| • FRAME RATE: | 500/s | 5000/s |
| • RESOLUTION: | 256 X 256 | 1024 X 1024 |
| • FILTER STORAGE: | 500 TARGETS | 2000 TARGETS |
| • DATA RATE: | 500 MOPS | 100 GOPS |
| • SIZE(OPTICAL HEAD): | 100 cm ³ | 10 cm ³ |

Table I Comparison Of The Performance Of BPOF Optical Correlator And Electronic Implementation

B.3 Antisubmarine Warfare

Passive detection systems based on electronic processing of acoustic hydrophone sensors is one of the established methods of carrying out ASW. However, the threat of acoustically quieter enemy submarines dramatically increases the demand for improved ASW hardware to ensure an adequate underwater surveillance capability. A hybrid of electronic and optical subsystems is the only way to satisfy these data-rate requirements because advanced ASW surveillance hardware will need a computational rate up to 10^{14} ops/s.

To remain covert, passive ASW systems do not use an active source, but detect the acoustic waves of enemy submarines imbedded in the combined background signals of nearby ships, surface waves, and distant storms. The composite acoustic signal is passively detected by arrays of hydrophone sensors. The signals range in frequency from about 5 Hz to 45 Hz and ASW hardware splits the acoustic wave spectrum into frequency "bins." To analyze the frequency spectrum data for target identification-and-location requires computationally intensive adaptive coherent matched filter techniques for target location and identification.

The total volumetric field handled by passive ASW systems is divided into cells, called voxels -- the smallest resolvable volume of ocean water that can be detected. For example, about sixty six million voxels are contained in a surveillance volume of 1000 km by 1000 km by 1 km. Coherent processing of the signals, from all the voxels as measured by the output of all the frequency bins of all the hydrophones in the array, involves inverting a matrix of numbers, and an estimate of the order of the required computational rate is obtained from the following relationship:

$$\text{Computation Rate} = \frac{LMN^2}{\Delta t}$$

*Where: N = Number of hydrophones
L = Number of frequency bins
M = Number of voxels
 Δt = Frame time period*

Today's ASW passive systems use about 400 hydrophone sensors. More sensitive ASW systems are needed to meet the future threat of very quiet enemy submarines. To achieve this capability requires increasing the number of hydrophone sensors. However, the sensitivity, as measured by the signal-to-noise ratio, only improves as the square root of the number of sensors. Therefore, to increase the sensitivity by 10 dB requires one hundred times the number of sensors and ten thousand times the number of computations. Plans are being made to build high-gain ASW systems that use from 3000 to 300,000 hydrophones. Digital silicon computers may not be able to satisfy the upper limits of an ASW projected requirement of 10^{11} operations per second, and certainly will not be able to provide the additional computational power to further improve the signal-to-noise ratio.

From the above considerations, the projected silicon logic devices may not be able to provide future ASW hardware with large computational capabilities. An example of a recently developed

commercial optical component that has the potential for high computational performance is one based on a hybrid semiconductor structure consisting of a self-contained, voltage-controlled light absorber and photodiode within the same structure. This self-electro-optic device (SEED) combines electroabsorption with detection to produce efficient, high-speed, low-energy optically and/or electrically controlled devices. The most attractive device in this class is the symmetric self-electro-optic effect device (S-SEED) which utilizes two SEEDs in a complementary configuration, as shown schematically in Figure 5. This device has the advantage of insensitivity both to laser beam power fluctuations and to biasing. Potential applications for S-SEEDs not only include optical computing elements for ASW, but also may be used for optical correlators, free-space reconfigurable interconnects, modulators, three terminal devices (field effect transistors:F-SEEDs), detectors, and dynamic memory elements.

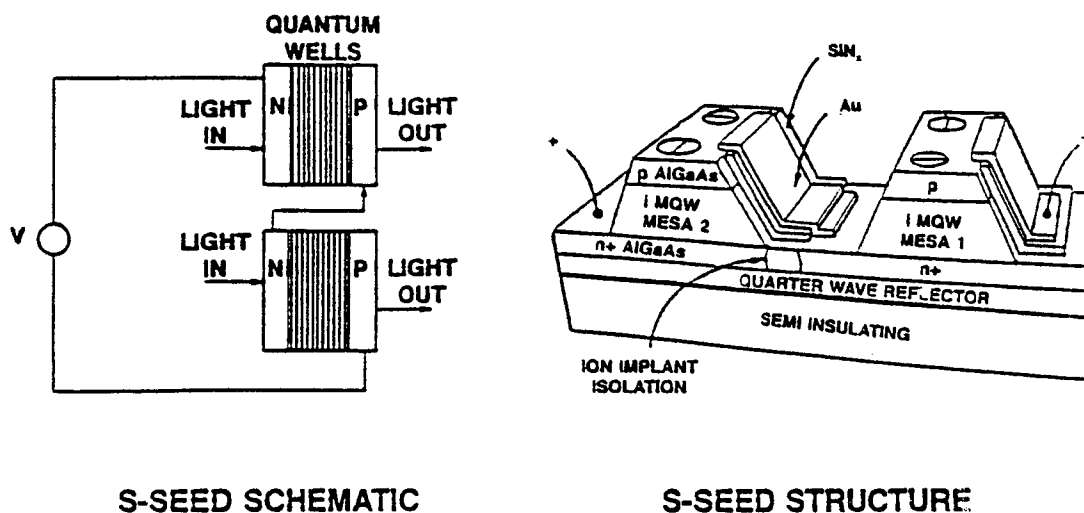


Figure 5 Symmetric Self-Electro-Optic Effect Device (S-SEED)

A SEED is a bistable device and has one state in which an applied voltage shifts the absorption edge to make the device transparent. A short pulse of intense light can then toggle the device to the other "off" state. By reducing the voltage across the device, the absorption shifts back and allows the standby beam power to hold the state.

The present and projected speed-switching energy tradeoff of SEEDs is shown in Figure 6. Commercial S-SEEDs are currently produced as 32x64 element arrays with switching speeds of 1 nanosecond and switching energies of 2.5 picojoules. The optical switching energy is essentially that energy necessary to charge the capacitance of the device. Research grade devices that switch in 33 picoseconds, with a switching energy of 17 picojoules, should be commercially available by 1995. At low operating bias voltages, switching time increases and switching energy decreases. Device arrays operated in this mode might be used in optical memories, in optical correlators for image processing, or in other areas where minimal power per element is required. In areas where a fairly

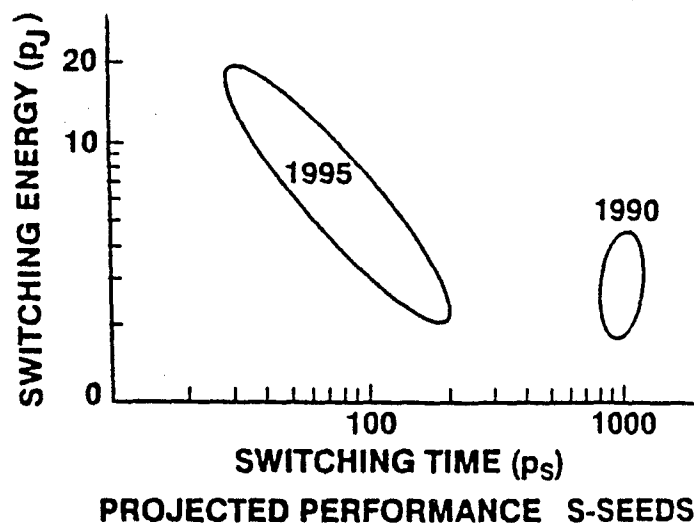


Figure 6 Projected Performance Of S-SEEDs

low density of devices is required, the devices could be operated at a larger bias voltage with a consequent increase in speed and power dissipation. Applications for this mode might include ASW optical logic elements or optically reconfigurable interconnects. In the future, one would expect larger arrays (256 x 256) with smaller device geometries and lower switching energies. More sophisticated logic functions can also be expected.

AT&T demonstrated a proof-of-principle of an optical digital processor using four arrays of 32 S-SEEDs illuminated by two 10-mW laser diodes. The optical architecture was arranged to allow the laser diode beams to connect with the arrays in free space using external lenses. It was demonstrated that because of the intrinsic parallelism of the architecture, 32 channels of information were able to be processed simultaneously at a 1-MHz rate. The research at AT&T is directed to the on-going development of hybrid S-SEED switching components. The device feasibility was demonstrated in a laboratory optical digital processor system.

Another example of an approach that might be used for ASW applications is one underway at OptiComp for a programmable general-purpose optical digital computer using off-the-shelf laser diode arrays, lenses, channelized AO Bragg cells, and silicon avalanche photodiode arrays. The main thrust of this activity is to exploit optical connectivity and the natural AND-OR-INVERT logic provided by an optical architecture. A prototype optical computer was built using two cascaded 32-channel tellurium dioxide AO Bragg cells. The essential feature of the system is the use of the photodetector as an OR gate and the cascaded AO cells as AND gates. The photodetectors function as a digital device to determine the presence or absence of a laser beam and is not used as a threshold-level detector as is done in the spectrum analyzer optical architecture.

In the OptoComp implementation, the AND logic is derived from the laser beam passing through two cascaded AO cells which is either absorbed or transmitted depending on whether the transmittance of the pixels of the AO cells are "on" or "off." The natural parallelism of optics allows for the expansion of a planar array of AO cells and detectors to a three-dimensional architecture of SLMs by the use of cylindrical lenses to focus the channels of light onto an array of detectors. The optical central processor unit performs as a reduced instruction set computer (RISC) and is projected to perform 12.8 billion 64-bit midterm calculations per second which is equivalent to about 8×10^{11} operations per second. The input/output rate is 3200 bytes per second.

Figure 7 is a projection of how an optical subsystem processor composed of SEED architectures or the OptiComp Digital Optical Computer (DOC2) computer may be able to satisfy future ASW requirements. For comparison, the computational rate of a CRAY IV computer is shown as an indication of the limitation of an all-electronic computational approach.

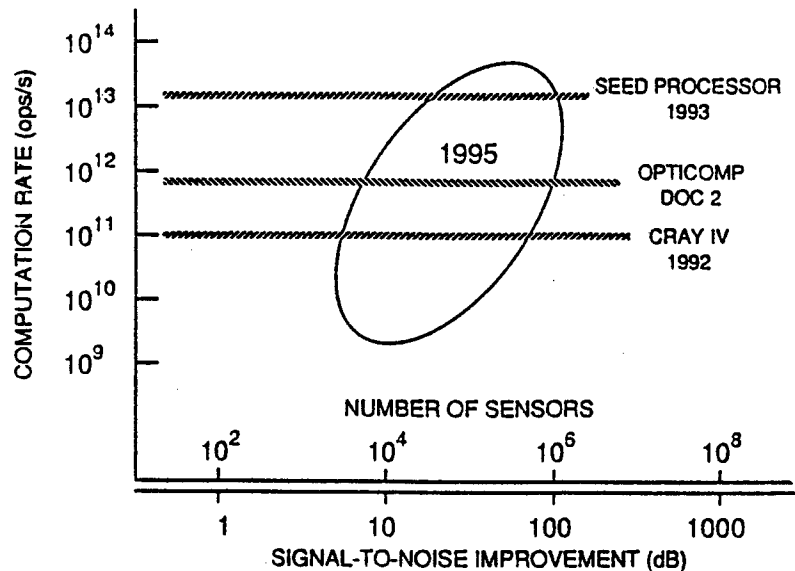


Figure 7 Computational Requirements Of ASW

B.4 Multispectral Analysis

NASA recently determined the anomalies of the burn characteristics of the exhaust plume of the Space Shuttle main engine by performing a computationally intensive process of multispectral analysis. It is projected that a computational rate of three hundred million ops/s will be required to analyze 2090 spectral bands of the exhaust plume at a rate of 1000 frames per second. This data rate must be provided by onboard hardware to enable the precise and rapid identification of the mass flow rate of different elemental species in the plume for purposes of engine operational control.

In addition, future NASA observing satellite hardware will require high-rate multispectral analysis to generate detailed high-resolution spectral maps of the ground. The required computational rate of 300 tera ops/s is so large that future silicon electronic devices may not be able to satisfy the logic switching speed. In this application, the problem is to determine the spectrum of the mineral species present from the data of an imaging sensor. NASA is formulating plans to construct a high resolution spectrometer that will analyze 192 spectral bands from one million pixels at a rate of five frames per second. To provide this high computational rate, one approach is to formulate the problem as an optical neural network in order to provide the large number of interconnections and parallel computation needed for a solution. In addition to the advantage of speed derived by parallelism, this approach also provides a computational scheme capable of learning from examples.

Figure 8 shows how optical neural network development in the near term and in five years may satisfy typical NASA mission requirements. Current activity is based on a liquid crystal light valve CRT and a 1D 256-element Bragg cell, and future 2D Bragg cells with 64 x 2048 elements will be able to satisfy NASA's long-range computational needs.

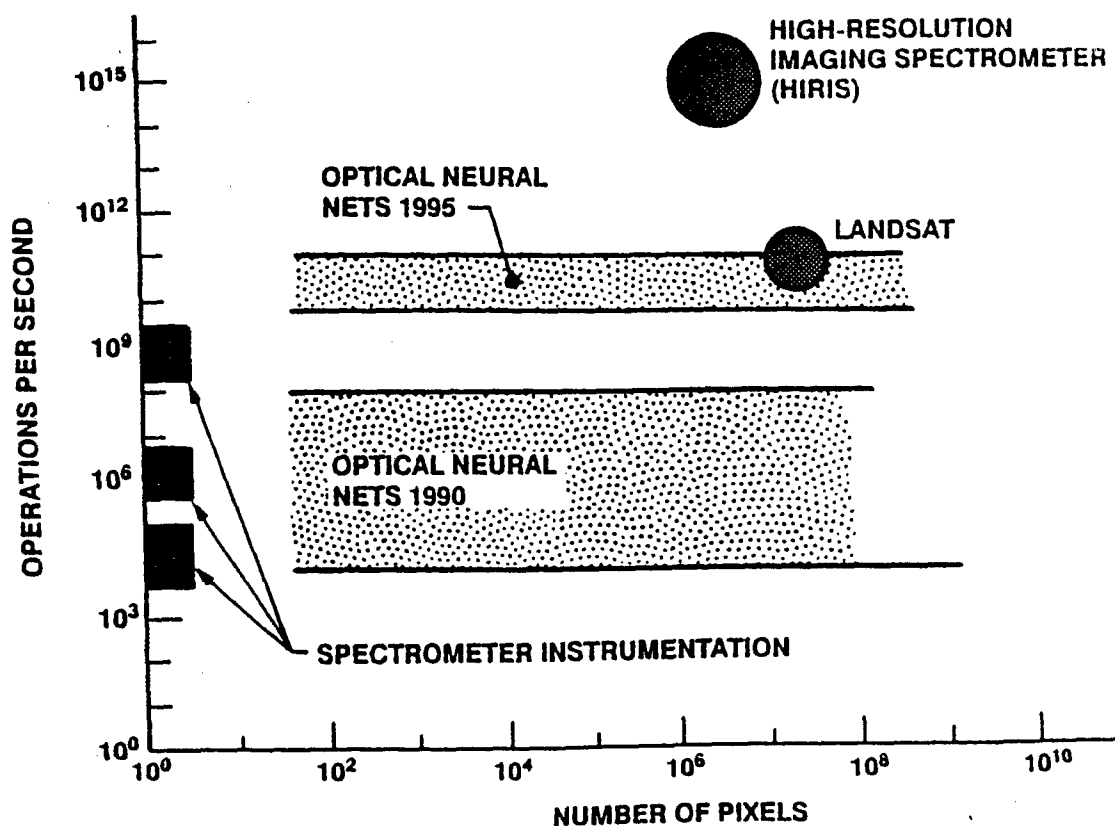


Figure 8 Typical NASA Mission Requirements Versus Optical Capability

A wide range of different experiments is now being carried out to understand and verify the candidate approaches to implement artificial neural networks. Neural networks are trained to produce

a desired response from input data by altering the strengths of the connections between the neurons of the network according to a learning algorithm. One of the attractions of neural networks is their ability to perform decisions on input data without the need for a precisely defined computer program. This feature is inspired by the operation of the human brain and makes artificial neural networks ideal for problems such as multispectral analysis which requires classifying a range of inputs into general categories.

Artificial neural networks are massively parallel computational systems composed of interconnected planes of neurons. Figure 9 illustrates a three-layer system consisting of an input plane, an output plane, and a hidden plane. This architecture does not have a central controller, but consists of a large number of analog processing elements (neurons) that are densely interconnected with feedforward and feedback paths. In addition, the interconnects among the processing elements may be fixed or dynamically changed.

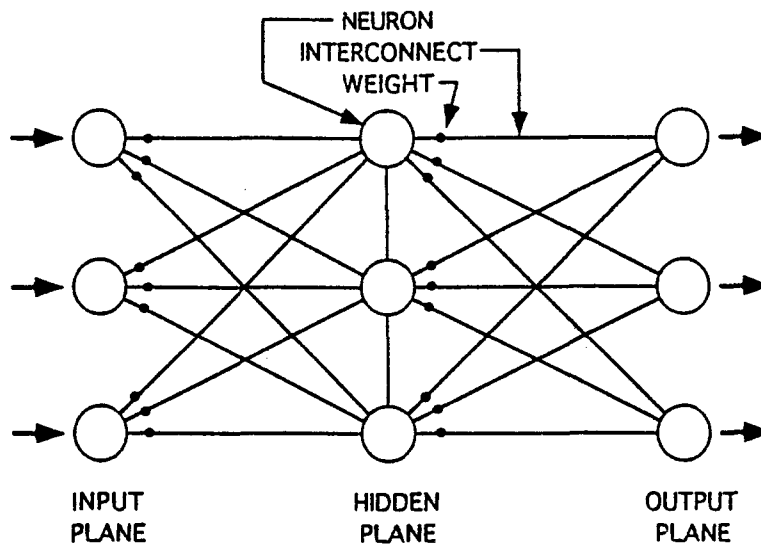


Figure 9 Three-Layer Artificial Neural Network

Each neuron of a neural network may have a linear or nonlinear threshold transfer function. The nonlinearity in turn may be smooth or a step function. In addition, the dynamics of the weight of each neuron constitute classes of learning rules such as (in the order of complexity) Hebbian, Widrow-Hoff, perception, etc. For example, the Hebbian learning rule states that when the activity of a particular neuron is correlated to the activity of another neuron, then the weight between the neurons should be strengthened. This rule has been used to develop associative memory systems which are content-addressable memories that can recall complete noise-free objects when addressed by partial or distorted input objects.

Experiments in artificial neural networks have been carried out along three lines of research: the simulation of uniquely neural network learning algorithms on conventional digital computers, the

application of non-neural-network algorithms on neural networks, and the use of neural network algorithms on neural-network architectures. The third category is the most promising use of optics in neural network implementation.

A good example of a neural network implementation is being developed by Hughes: an associative memory neural network that is a hybrid of optical and electronic techniques that falls into the third category listed above. Optics was chosen because of the availability of natural and easy interconnections and parallelism. In the experimental setup, a host electronic computer only performs the table lookup function to compare the output optical neural plane to a stored reference. The neural network consists of a liquid-crystal-light-valve CRT which illuminates a 2D neural plane. Neurons are distributed in this plane so that the active state of each neuron is represented by the relative intensity of a spot of light. The CRT detects a threshold level of each neuron for comparison to a library of stored data contained in the host electronic computer.

In the Hughes implementation, the interconnections among the neurons and the weights associated with the neurons are provided by a 2D hologram SLM which is able to store a sinusoidal diffraction grating produced by the interaction of two beams. The depth of modulation of the sinusoidal diffraction is proportional to the intensity of the beams and resembles a Hebbian learning rule. Interconnection among neurons is provided by Bragg diffraction of the beams which form a cone of allowed interconnect paths. In this architecture, a specific path is chosen by using techniques of self-pumped phase conjunction. Hughes has reported the development of a 64x64 optical neural network and the demonstration of the interconnection of 300 neurons. In this approach, a neuron is represented by a spot of light and is interconnected to other neurons by a 2D hologram SLM. Hybridization results from the use of a host electronic computer to allow the neural network to compare its output to a library of possible stored configurations.

In a research program at MIT Lincoln Laboratory, another approach is based on the integration of III-V materials in a 2D optoelectronics SLM architecture. This implementation uses optically bistable GaAs MQW SEED structures that are integrated with other electronic devices on a single chip. Instead of using an external battery and resistor, the SEED employs an electronic tunnel diode. The characteristic of the tunnel diode is chosen to control the type of optical bistability required such as a fast action "snap" optical input/output function. The MIT group has produced integrated optoelectronic neurons consisting of a layer of 20-micron pixels composed of resonant tunnel diodes, FET channels, MQW modulators/detectors, and dielectric mirrors. An advantage of the hybridization at the chip level is the use of a local chip-to-chip electrical interconnection as an inhibition function for contrast removal. Research is planned for multilayered planes of optical neurons having contrast detectors with oriented receptor fields for military applications such as ATR boundary segmentation in the presence of noise.

Research in optical neural network computations is emerging at a fast pace and this activity underscores the potential of hybrid optical/electronic architectures in performing computation functions normally associated with electronics.

B.5 Applications Requiring High-Speed Switching and Connectivity

Plans have been formulated for a Federal High-Performance Computing program to enable NASA to study deep-space exploration and DOE to carry out research in fusion. In support of this program, Thinking Machines Corp developed the "connection machine" which provides high-speed

digital computation from a massively parallel architecture of a large number of interconnected microprocessors. The feasibility of interconnecting 64,000 microprocessors was demonstrated and it is planned to increase this number to one million. The computational speed of the "connection machine" is limited by cross talk on the interconnecting copper wire coax cables. This places an excessive design burden on isolating the connecting channels. In demonstrating the potential of optics, Honeywell in a DARPA-sponsored program, was able to use fiber optics as interconnect channels of the "connection machine" at a bit rate of 10^9 bits per second. Optics, because of its natural parallelism, noninterference and intrinsic high speed, will be able to solve the interconnect problem of future massively parallel machines.

In addition to fiber optic data communications, there are other optical approaches that may be able to exploit optics for its characteristic parallelism, high-speed, and noninterference. Figure 10 illustrates the switching speed and connectivity capabilities of SLM opto-electronics integrated circuit (OEIC) and SEED technologies. In the figure, the performance of Si/GaAs switching devices is shown limited to about 1000 pin-outs per chip or pixels/cm².

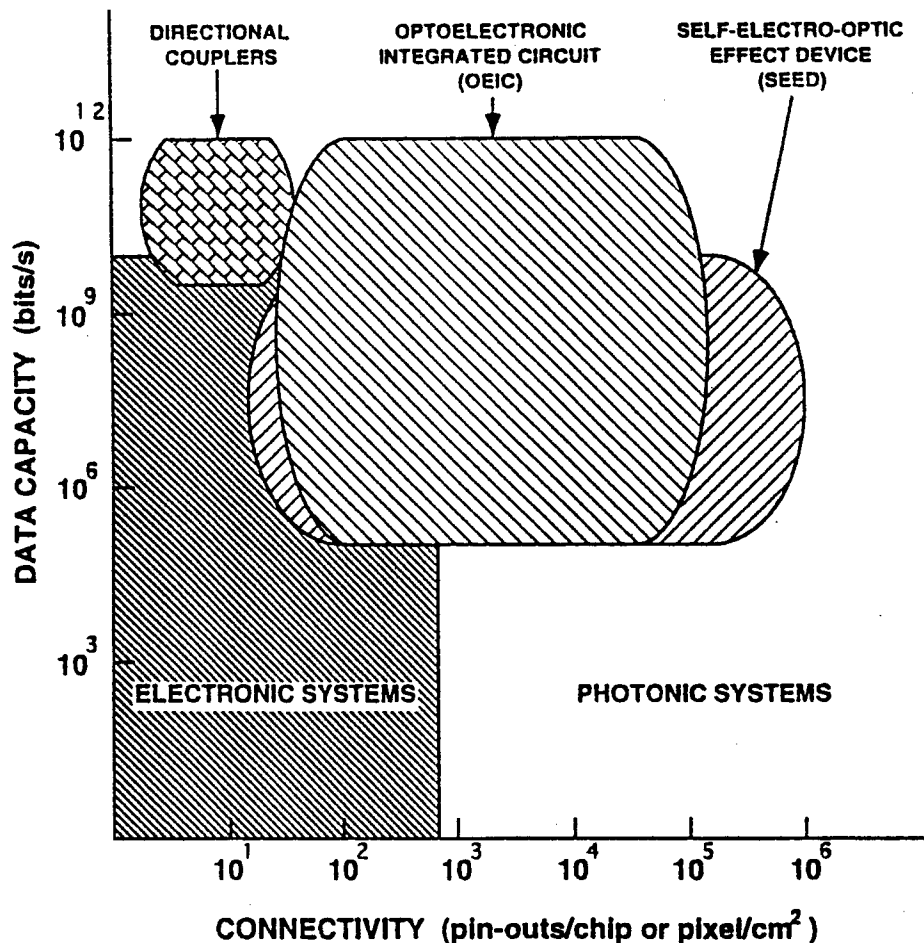


Figure 10 Optical Switch Device Capability

(This figure adapted from an article by Scott Hinton, IEEE J. on Selected Areas in Communication, 1988, p.1220.)

The OEIC and SEED SLM technologies are two examples of optical devices that have the potential of meeting the demands of future military systems for high-speed processing. The OEIC utilizes optical channel waveguides in a single monolithic structure to integrate light sources, modulators, detectors, and other devices into functional switching circuits. Cross talk as low as 20 dB has been achieved. It is projected that OEICs will be able to operate at 10^9 bits per second by 1993. The SEED, which was described in section B.3, has demonstrated a switching capability of 10^9 bits per second in a 100-channel configuration and has the potential of providing connectivity to 10^6 pixels per cm^2 . The 1995 projected performance of the SEED switching speed and required switching energy is shown in Figure 6.

For applications that need good connectivity and high-data-rate capacity, the optical logic etalon (OLE) device, based on all-optical bistability, is a good example of a candidate technology. This device is different from a SEED because a SEED is a type of optically bistable device that uses external electronic feedback. In essence, an electrical signal from the device is fed back to alter the light transmission of the device. In contrast, the OLE switching device uses only optical bistability. Typically, these devices employ a Fabry-Perot etalon with an index of refraction that responds nonlinearly to light. Feedback occurs optically within the etalon material itself. This type of bistability is based on an optical cavity that is detuned far enough from the wavelength of a laser light source to make it reflective at low light intensity in an "off" state. At high light intensity, the transmission maxima of the cavity are shifted to the wavelength of the laser, increasing transmission and producing a further shift in wavelength, thus allowing the device to be turned to an "on" state. Research has been ongoing in the development of GaAs etalon bistable devices for switching applications. Since all-optical bistable devices are at the fundamental research level, practical devices probably will not appear in the next five years.

C. Optical Versus Electronic Interconnections

1. Optical Channel Waveguide Interconnects

The projection of the power needed for both electronic and active-optical interconnects versus data rate is shown in Figure 11. The power per interconnect includes electrical output driver power, the power dissipation in the transmission line, and the detector power needed for optical interconnects. Due to power limitations, CMOS interconnects will not be able to operate beyond a data rate of 200 MHz, and ECL interconnects will be limited to less than 4 GHz. In contrast, at a 100 MHz data rate, active polymer optical interconnects now need an order of magnitude less power per interconnect than CMOS at 100 MHz, and will require less power than electronic interconnects at higher data frequencies.

For CMOS, energy per bit is constant and the required power is linear in bit rate until the ability of the transistors to supply the required current is exceeded; then the curve rises more steeply. For terminated transmission lines such as Si or GaAs ECL, power (not energy per bit) is constant. The level of 80 mW is for an assumed 2-V signal into a 50-ohm terminated line. The required power is essentially length independent for typical interconnection lengths of a few cm or less. At high bit rates, the curve rises because the transistors become stressed to swing the current at the higher rates. In this regime, the energy per bit becomes nearly constant.

Optical interconnections have a length-independent power that tends to approach a constant energy per bit at high rates. The power required is relatively insensitive to whether an optical source

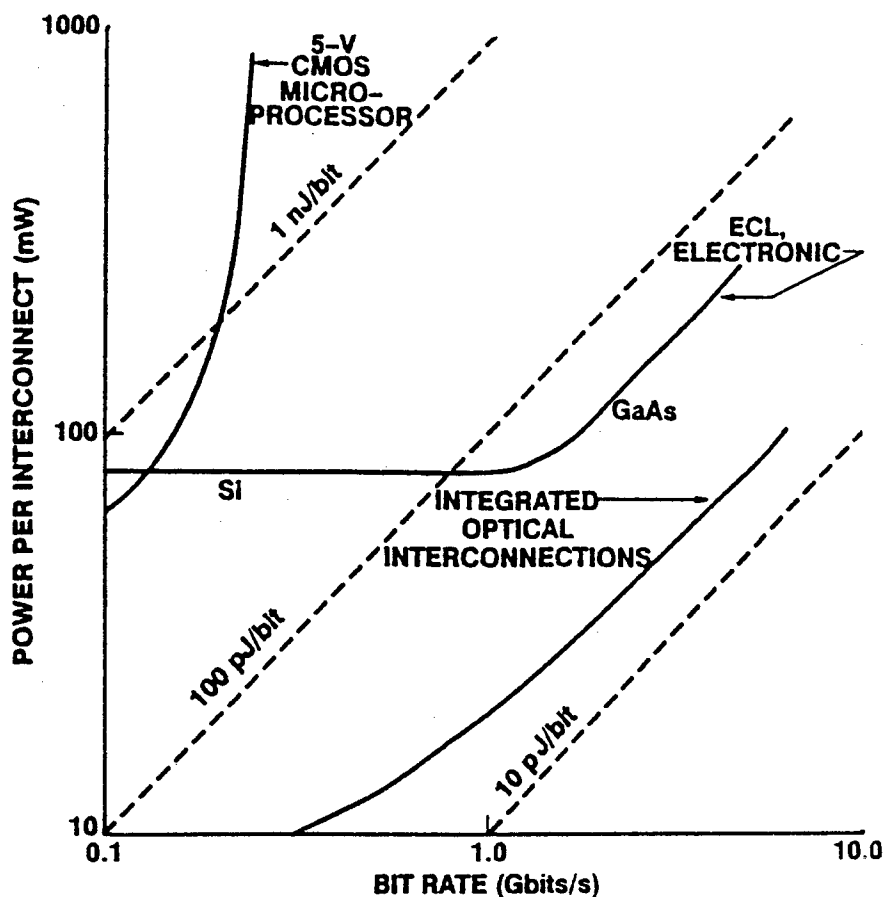


Figure 11 Power Requirements For Digital Interconnections

(e.g., a diode laser) or a separate modulator is driven by the bit pattern. At lower bit rates, the energy per bit is higher because of the power needed to reach laser threshold and the minimum operating power of optical sources.

When special optical detector-to-digital circuit interfaces are employed, optical interconnections promise lower power than electrical interconnections. In addition to power savings, optical interconnections have superb immunity to electromagnetic interference (a major constraint on electrical interconnections at high bit rates), provide the means for interconnections free from quasi-planar constraints, and allow a high degree of parallelism.

2. Optical Free-Space Interconnects

Figure 12 illustrates how the surface emitting laser (SEL) will be used in 2D SLM arrays for matrix processing. The SEL structures, as shown in Figure 13, have a small active volume and a short optical cavity that promise a capability for low threshold current and high-speed modulation. Currently, the threshold currents are about 0.3 mA, output power is about 0.5 mW, with differential quantum efficiency near 25 percent, and the demonstrated modulation speed of 8 GHz, with much higher speeds possible.

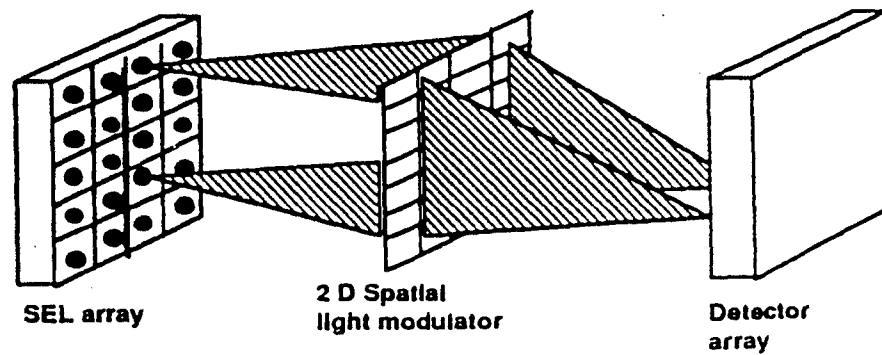


Figure 12 A SEL Optical Matrix Processor

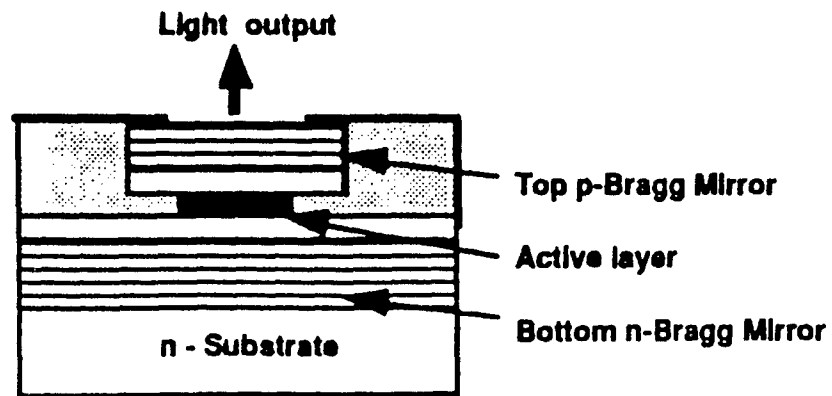


Figure 13 A Typical Vertical Cavity SEL Structure

With the fast pace of the research effort, in the next five years a SEL should be developed with a threshold current of about $10\ \mu\text{A}$, a power output of $2\ \text{mW}$ at a drive current of a few mA , and a differential quantum efficiency of 80% . Also, the modulation speed is expected to reach about

| | Current Status | Projected (1995) |
|-------------------------------|----------------|------------------|
| Threshold Current (CW) | ~ 0.3 mA | ~ 10 μ A |
| Differential Efficiency | 25 % | 80% |
| CW Power Output (@ 1.5 mA) | 0.5 mW | ~ 2 mW |
| Modulation Frequency | 8 GHz | 50 GHz |
| Array Formation | 32 x 32 | 1000 x 1000 |
| Optoelectronic Integration | not available | available |

Table II Vertical Cavity SEL Performance

50 GHz with proper packaging and circuit arrangements. Low threshold current and high efficiency operation of SELs are very important for high density, parallel optical processor, and neural net applications that require large SEL arrays. The inherent planar structure of SELs allows easy fabrication of 2D arrays. So far, small-scale SEL arrays of 32 x 32 elements have been demonstrated with a corresponding device density of 2 million per square cm. Larger SEL arrays of 1000 x 1000 are realizable within the next five years based on the current technology. However, the key issue will be the device uniformity and fabrication yield of such a large array. Table II reviews the current and projected status and performance of the vertical-cavity SEL as applied to free-space interconnects for HSOP applications.

Monolithic opto-electronic integration of SELs has not been demonstrated as yet, but is expected within two years. Such an opto-electronic integration technology may provide a solution to the array addressability issue. Monolithic opto-electronic integrated SEL arrays with individual addressable capability should also be realized by the 1995 time frame.

D. Optical Versus Electronic Memory Capability

Data storage systems have advanced along three distinct lines of technology: the solid state silicon chip, the traditional moving magnetic storage media, and the recently emerging optical storage approach. Performance of all these technologies is currently improving, requiring periodic evaluation of new storage devices for possible use in military systems.

Many factors determine the type of storage media for a particular military application, but the dominant ones are access time, capacity, transfer rate, cost, and physical size and weight. Figure 14 shows the current and projected development of solid-state silicon, magnetic, and optical storage devices from the standpoint of access time and storage capacity. Currently, the rotating magnetic disk competes with the rotating optical disk for the ability to store large quantities of data. The optical

rotating disk falls into two categories: the prerecorded compact disk read-only memory (CD-ROM) disk and the write-once, read-many (WORM) disk. Both use a laser to store bits of information as pits on the surface of a recording media and are technically attractive because they can store more data in a smaller space of the recording media than on a magnetic disk. Moreover, CD-ROM and WORM disks are removable and can achieve further storage capacity by using more than one disk in a "jukebox" configuration. Although CD-ROM and WORM disk drives provide greater capacity, they are not erasable, are bulkier, slower, and need more power than magnetic disk drives. Because of this limited functionality, it is difficult for current optical devices to compete in price, speed and the ability to rewrite.

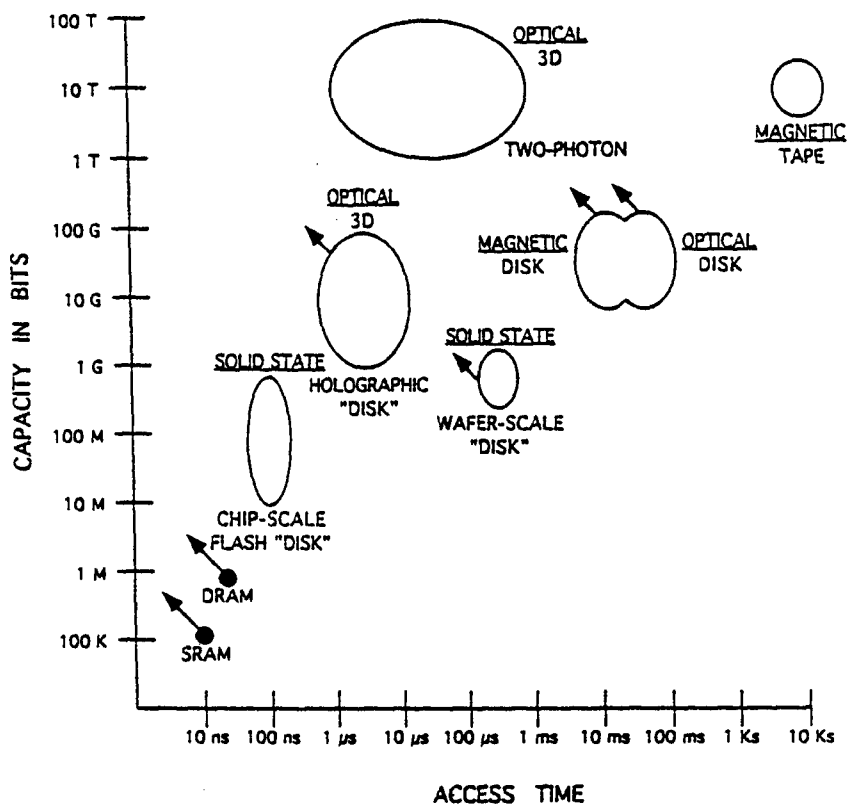


Figure 14 Memory Capacity Versus Access Time

To circumvent the limitations of the CD-ROM and WORM optical disk, an optical disk that can be erased before rewritten was recently marketed by the Japanese that uses a hybrid magnetic-optical (MO) technology. In this approach, a two-pass process is used to write a single bit on the disk. In the initial erase pass, a laser heats a spot on a rare-earth transition-metal rotating media to the Curie temperature where the magnetized substance loses its magnetic orientation. Once this temperature is reached, in a second pass, an electro magnet at the spot generates a magnetic field to produce a new magnetic orientation. As the spot cools past the Curie temperature, this new magnetic

orientation is stored and read optically using the Kerr effect. In the read process, the direction of the rotation of polarization of the read laser beam reflected from the surface depends on the magnetic orientation of the spot on the surface. Negative Kerr rotation represents a stored "1" state and positive rotation a stored "0" state.

The MO disk technology has the potential for large capacity erasable data storage, but the two-pass erase/write process effectively doubles the write time. Another limitation is the small magnitude of the Kerr rotation, about one percent, requiring a more sensitive read head made of larger optics. The access time of the MO disk is larger than the magnetic disk because of more massive optics which increases the write time and reduces the transport speed of the read head.

In an attempt to develop an optical disk that can be written in one step, an all-optical process was developed based on a phase-change of the recording media. This technique uses a laser to change a spot on a tellurium thin film from the crystalline to amorphous state and back again by switching the temperature of the spot between its glass-transition and melting point. In this technique, an 8-mW laser beam changes the spot from the amorphous to the crystalline state, and an 18-mW beam raises the temperature of the spot to the melting point which then cools to the amorphous state by revitrification.

Optical disk phase-change technology has resulted in a marketable mass storage system having a storage capacity of 400 Gb in a jukebox automatic cartridge changer. Each cartridge is on a 5-1/4-inch media and stores 8 Gb of data. Although this technology has a high-performance storage capability with improved access time compared to the WORM, an average access time of 90 ms is still about 10 times slower than the magnetic hard disk drive.

A complete departure from 2D optical rotating disk technology is optical volume memory that stores data in three-dimensional (3D) media, thus introducing a third storage dimension in the same volume. There are two prominent developments in this area: one stores data as a hologram in photorefractive materials, and the other uses a two-photon absorption mechanism to store a single bit of data at separate locations throughout the volume of a photochromic material; both techniques use the SLM as the interface between the host computer and the optical storage media.

Holographic 3D data storage technology is based on the use of arrays of crystallite fibers of strontium barium niobate to store data in a very small volume. For example, a 50 x 50 array of fibers occupies a volume of 5 cm by 5 cm by 0.5 cm. Bulk photorefractive material is not used in this application because of destructive read-out mechanisms, and the difficulty of producing large bulk photorefractive material of high quality. The data storage system uses a SLM to convert an electronic bit pattern to a spatial array of light and dark spots. The Fourier transform of the SLM spatial bit pattern is generated and combined with a reference laser beam to produce an interference grating stored at one of the crystallite locations capable of holding 30 to 50 optically formatted "stacks" of "pages" of 64 kb of data per page. To write another 64 kb page in the same stack, the angle of the reference beam is shifted about one-fourth of a degree. Data are read from the hologram by addressing the reference beam to a specific stack and adjusting the angle of the beam to retrieve a specific page. The resulting spatial bit pattern is focused on a CCD detector array to reconstruct the electronic bit pattern.

In the alternate two-photon 3D absorption approach, photochromic spirobenzopyran molecules within the volume of a thin film media are optically addressed by the overlap of orthogonal laser

beams that excite a single molecule to an electronic state of higher energy. Using two-photon absorption, a bit is written only to one molecule within the crossed laser beams because a photon from one beam first excites the molecule to a virtual state and then a temporally and spatially coincident photon from the second laser beam further excites the molecule to a final real excited state. Reading the stored bit is based on two-photon-induced fluorescence and has the potential of extremely short access time because the change in energy level occurs in the picosecond range. The access mechanism of the two-photon storage and retrieval process is intrinsically short; however, it is the SLM interface between the host computer and storage media that determines the overall storage system access time capability. Improvements in SLM technology will have a profound effect on mass optical storage developments.

As shown in Figure 14, mass optical storage has the potential of providing a capacity of from one gigabit to about 100 tera bits, but the access time is currently limited to about 1 μ sec because of the SLM interface between the electronic and optical modules that make up the system. Improvements in the performance of SLMs continue to take place, and parallel developments in both chip-scale and wafer-scale solid-state mass storage "disks" are occurring to provide the high-capacity storage with short access time needed in the near term.

E. Compact Spatial Light Modulator - A Critical Component

Hybrid optical/electronic hardware to meet future military requirements is limited by the ability of compact SLMs to provide high data-rate throughput. The two basic modes of programming a SLM are either parallel, using optics, or serial, using electronics. Serial programming is more compatible with existing support hardware, and most practical for near-term implementations, but parallel addressing could ultimately provide higher frame rates. For applications that use optical correlators, only the phase information (see Section B.2) is by far the most important, and thus only the four SLMs that accommodate this requirement are compared.

The state-of-the-art of the four parallel and serially addressed phase-only classes of SLMs are shown in Figure 15 along with their capability projected to 1995. The SLM capability is plotted in terms of the space-bandwidth product (pixel count) and frame or reprogramming time. MQW SLMs have not been included because they do not provide the required phase-modulation sensitivity for optical correlation applications. MQW devices are particularly applicable to high-speed digital optics applications, where low-contrast amplitude modulation only is acceptable. The capability of the serially addressed SLMs is limited by the speed of the electronics because the space-bandwidth-product divided by the frame-time constrain the overall performance, as shown by the straight line on the 1995 projected capability.

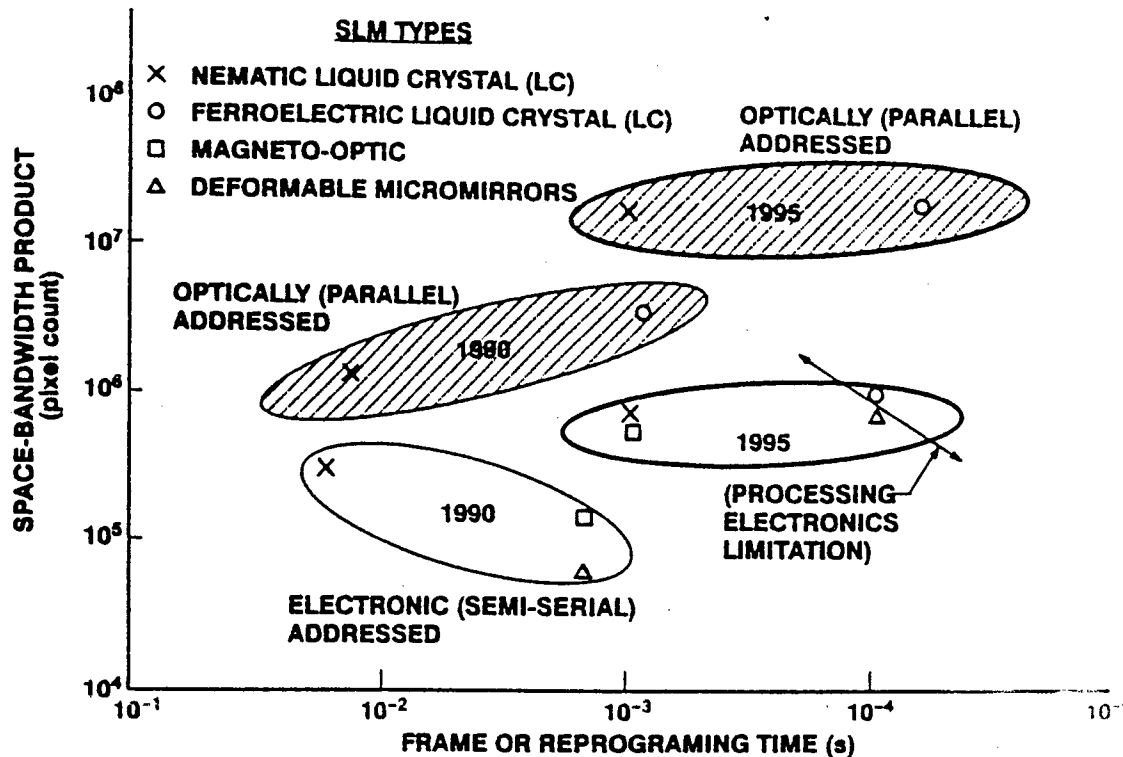


Figure 15 Compact SLM Projected Capability For Optical Correlators

II. WHAT MAKES OPTICAL PROCESSING DESIRABLE?

The development of high-speed optical devices and subsystems, and their use in a variety of hybrid applications is a subject of intense research supported by DoD, DARPA, and NSF at many universities and industrial laboratories. These efforts are strongly motivated by the success of key demonstrations of this emerging technology. A synopsis of the technical status of some prominent HSOP devices, and the results of their successful use in selected demonstrations is shown below. It is these demonstrations that have stimulated interest in HSOP and provide the reasons why optical processing is desirable. The following is an overview of these developments.

- Commercially promoted, low-cost 300-Mb/s fiber-optic subsystems are now used in low N applications to interconnect electronic digital computer modules, back-plane, and board-to-board subsystems. Extending this technology to higher data rates for commercial applications has been limited because of the high cost of the optical subsystem. DARPA is trying to stimulate commercial activity by funding the development and demonstration of 1-Gb/s-rate optical interconnection of parallel electronic processors. However, this technology has not yet been transitioned to the electronic digital community.
- DoD and NSF efforts have resulted in significant technical advances for the different classes of SLM devices which include acousto-optic, ferroelectric liquid crystal, magneto-

optic, micro mirror, and the recently developed MQW SLM. A three-order-of-magnitude improvement in processing performance is forecast for the next five years.

- DoD support has produced progress in the development of photodetector arrays, and significantly, AT&T manufactured prototypes that integrate MQW SLM and photodetector functions at the pixel assembly level.
- DoD funded programs have stimulated commercial interest in a variety of SEL arrays that are now routinely fabricated in the laboratory. Low power arrays of 1000x1000 MQW SELs on 20-micron centers have been demonstrated.
- The Navy has reported excellent results for a 1D channelizer that provides more than 2-GHz instantaneous bandwidth and more than 50-dB dynamic range.
- The Army showed that the use of a 2D optical binary, phase only, SLM in ATR correlation functions was able to recognize nine out of ten targets whereas the conventional electronic approach only recognized five out of ten targets. Based on this demonstration, it is predicted that the 1D channelizer capability will meet the operational requirements of many military users.
- An experimental commercial optical neural network using a ferroelectric SLM and a LCLV CRT as an algorithm testbed shows promise as a programmable associative memory. The feasibility for 2D image processing at 10^{10} ops/s was demonstrated.

The above highlights of HSOP set the stage for the acceptance of this new emerging technology by the developers of military hardware, but the transition to actual deployed systems must be formulated according to a specific plan.

III. Technology Push and Systems Pull of HSOP

The effective military use of an emerging technology must recognize the maturity of the technology relative to a "system pull" and the likelihood of an application being developed by the commercial sector. A perspective of the interplay of these forces is shown in Figure 16 and the rationale for ranking the dominant thrusts within the analysis matrix is as follows:

- **Signal Correlator:** Specialized Bragg cell AO signal correlators are being used in a mature technological niche.
- **Channelized Receivers or Signal Channelizers:** The current Bragg cell AO channelizer technology sees limited system use. Rugged, coherent versions can be available, in the near term, for system applications.
- **Optical Memories:** Compact optical disks are in commercial use and the wise strategy is to adapt commercial technology to DoD needs.

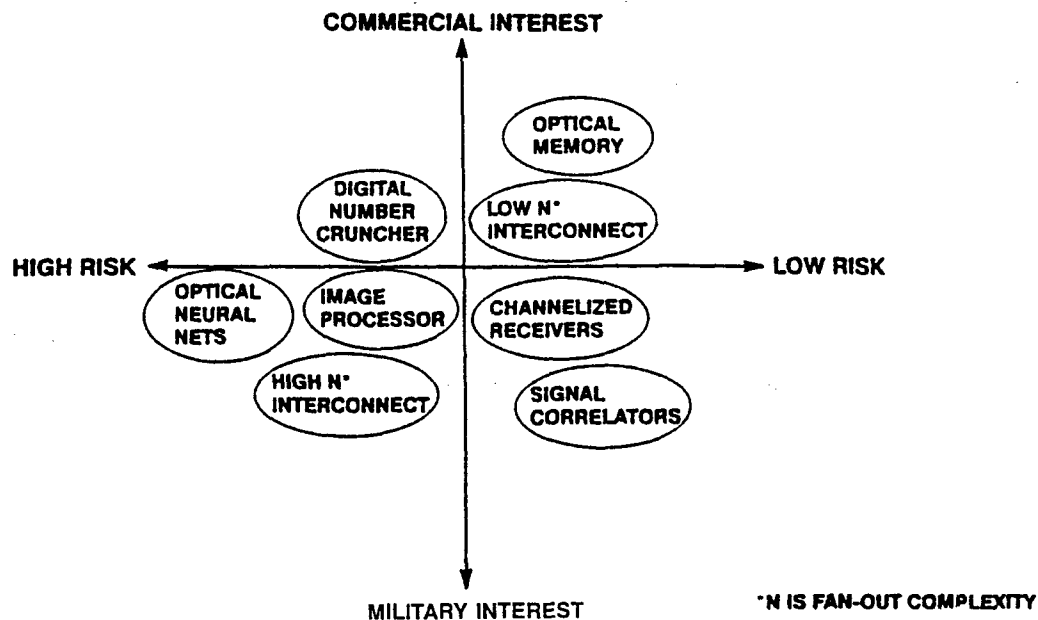


Figure 16 HSOP Application Perspective

- **Low N Interconnects:** This category includes optical interconnections with a fan-out of approximately less than 100. Board- and module-level development and crossbar switches are commercially desired.
- **High N Interconnects:** This category is for a fan-out of N greater than 100 and is principally oriented toward free space interconnect devices.
- **Digital Number Crunching:** Sometimes called digital optical signal processing, a non-neural network, totally digital processor is envisioned here. The state-of-the-art relative to competing silicon technology is immature.
- **Image Processor:** Silicon-based processor performance for ATR for picking out objects from background clutter is not yet satisfactory. Optical implementations offer inherent advantages.
- **Optical Neural Nets:** When practical architectures are proved successful, large fan-out optical interconnect implementations will be very important.

With reference to Figure 16, it is clear that strong technology base support is needed for technologies to the left of the center line.

IV. Government-Supported Programs In HSOP For FY 1990

Figure 17 is an estimate of government-supported programs in HSOP for the fiscal year 1990. The total funding level is \$45M and includes the 6.1, 6.2, and 6.3 categories.

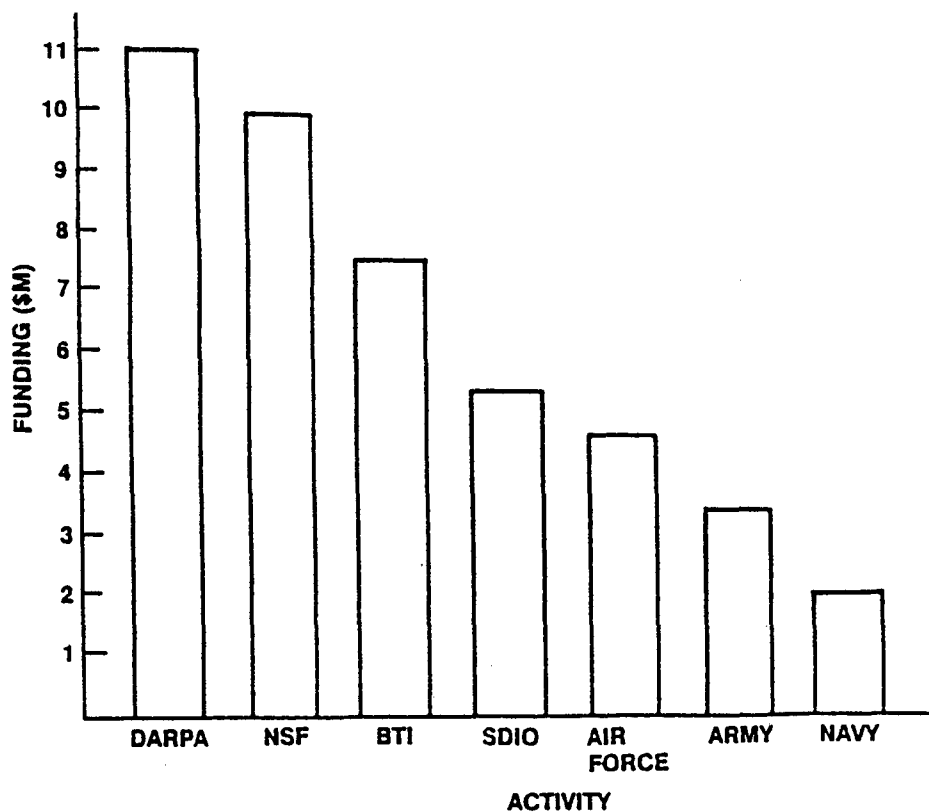


Figure 17 Government-Supported Programs In HSOP For FY 90

The technical thrusts of these programs are as follows:

- Algorithms for optical processing
- AO processors for ASW
- AO processors for communication
- AO processors for EW
- Image processing
- Pattern recognition
- Spatial light modulators
- Adaptive beam forming
- Correlators
- Detector arrays
- Digital computing with optics
- Symbolic computing
- Neural networks
- Interconnects

As a comparison, it is estimated that the U.S. industrial IR&D effort in these technologies for 1990 is \$75M.

V. U.S. Versus Foreign Effort in HSOP

The countries that have major efforts in optical device development that is relevant to DoD/NASA HSOP requirements is presented in Figure 18. This assessment is derived from the opinions of the industrial consultants and government Service members of Working Group C who have monitored the progress of the optical devices for several years.

| TITLE | U.S. | JAPAN | U.K./EUROPE | SOVIETS |
|--|------|-------|-------------|---------|
| BRAGG CELL CHANNELIZERS | ✓✓✓✓ | ✓✓✓ | ✓✓ | ✓✓ |
| OPTICAL MEMORIES | ✓✓✓ | ✓✓✓✓ | ✓✓ | ✓ |
| CROSS-BAR SWITCHES | ✓✓✓ | ✓✓✓✓ | ✓✓ | ✓ |
| OPTICAL NEURAL NETS | ✓✓✓ | ✓✓✓✓ | ✓✓ | |
| ANALOG PROCESSORS/ SPATIAL LIGHT MODULATORS | ✓✓✓ | ✓✓✓ | ✓✓ | ✓✓ |

**Figure 18 Qualitative Assessment Of The Relative Level Of Effort In HSOP
U.S. Versus Foreign**

An assessment of U.S. versus Foreign effort in HSOP is as follows:

- The U.S. continues to maintain a lead in the development of AO Bragg cell technology for advanced hybrid optical/electronic military signal channelizers. Japan, the NATO countries, and the former Soviet Union follow in their efforts, but it has been noticed that China recently demonstrated a Bragg cell with a higher efficiency than that produced in the U.S.

- The U.S. effort is on a par with the Japanese in the use of SLMs for analog optical processors.

- The Japanese lead the U.S. effort in the areas of optical memories, cross-bar switching for digital optical computing, and optical neural networks. Although the U.S. lags behind the Japanese in these areas, we are still well ahead of the NATO countries and the former Soviet Union.

VI. TECHNICAL ASSESSMENT

A hybrid optical/electronic processor is feasible because optics complements the strengths and weaknesses of electronic processors in certain niche applications. Optical technology is emerging in an evolutionary rather than revolutionary manner, and opportunities that require performance greater than 1 tera ops/s will best be met with a hybrid approach. However, unlike electrons, light does not interact with light and it is this characteristic that endows optical devices with a fundamental difference not found in electronics. Because of this basic difference, it is sometimes difficult to associate the relevance of HSOP as a transferable technology to specific military hardware. This disconnect often leads to problems in formulating a proper technical assessment. Part of the difficulty is the lack of understanding of the technical categorization of the emerging optical technology. To help solve this problem, an attempt was made to formulate the results of the STAR in terms of the broad generic categories of optical device developments and its use in potential military applications.

The diversity of the current development of HSOP devices may be appreciated from an overview of the government-sponsored programs given in Section IV. Although these activities are not technically focused, they do fall into three main generic architectural categories of optical subsystems as follows:

Optical Subsystems

- Analog
- Digital
- Neural Network

In addition, the following categories of candidate HSOP applications were used in a further effort to focus an assessment on the technical requirements of representative generic military systems.

Applications

- Spectrum Analysis
- ATR Pattern Recognition
- EW and ELINT
- Generic HSOP

Military Implementations

- 1D Correlators
- 2D Correlators
- Signal Channelizers
- Low N Interconnections
- High N Interconnections

The XSTAR was carried out to address those military users who have specific system requirements that must be satisfied. However, in assessing the potential of transitioning from device to system, it should be recognized that more than one of the above applications may relate to one HSOP subsystem.

HSOP is very desirable because it has excellent utility for niche applications. For example, a low interconnect (low N) fiber optic data bus between two digital data processors has a recognized value to users. This is a clear example of where optical device R&D and design approaches are able to improve a niche application performance level. Much less clear is the blend of niche applications requiring different architectures and device developments to satisfy user requirements.

Based on optical device performance projections presented in Section I, the following assessment of HSOP subsystems may be cited:

- Optical analog subsystems should see utility as "front-end" signal processors with dynamic range/accuracy limitations, but with special effectiveness in 2D correlation for ATR and also synthetic aperture radar (SAR).
- Optical digital subsystems have excellent interconnect virtues but suffer from reduced accuracy. New residue arithmetic methods or some other architecture peculiarly suited to optics is needed.
- Optical neural networks are unproven, and even though neural chips exist, total neural nets still remain to be demonstrated. However, neural nets seem to be particularly well suited to massive interconnectivity.

In many cases, silicon- and gallium-arsenide-based electronic processors or processor subsystems have strengths and weaknesses that are complementary to optical processor subsystems. Compact silicon-based vector processors for DoD systems that operate at about 10^{10} ops/s and massively parallel CRAY-type processors with more than 10^{11} ops/s are in development. However, limitations are starting to appear in the hardware capability (viz 10^6 channels) and in the software needed to code the algorithms.

In order to optimize the technical choices for future military systems, some sort of mixture of optical and electronic processing capabilities will be required. A hybrid optical and electronic processor is probably the right approach, but the specific technology mix depends on the application.

The SLM is a key optical component that will be used in future military systems. Some of the other key devices that pace the development of optical processor subsystems are: the laser source, fiber-optic interconnects, and detector arrays. In addition, other components such as cameras, fiber optics, conventional optics, binary optics, etc., also support the subsystem performance. It is the combination of all these devices used in a hybrid system that really establishes the speed, dynamic range, contrast ratio, accuracy, etc., since photon emission, detection, and modulation are controlled by electronics.

The time is ripe to force a union of optical research, electronic processor technologies, and processor architecture design. The fast pace of optical research and the recognition of electronic processor limitations support this conclusion. However, the job cannot be done without a focused hybrid development effort that is clearly based on the military user requirements.